Ministry of Higher Education and
Scientific Research - Iraq
University of Diyala
College of Artificial Intelligence
Engineering Technology
Department of Cybersecurity Engineering

الملحق 4: وصف المادة الدراسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Logic Systems**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☒ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	**CPE 104**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Cybersecurity Eng.		College	College of Artificial Intelligence Engineering Technology	
Module Leader	Dr. Ali Albu-Rghaif		**e-mail**	ali.alburghaif@uodiyala.edu.iq	
Module Leader's Acad. Title	Asst. Prof		**Module Leader's Qualification**	PhD	
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date	10/11/2025		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. To acquire the basic knowledge of Digital systems and applications. 2. To understand and examine the structure of various number systems and its application in digital design. 3. The ability to understand conversion between digital systems. 4. The ability to understand, analyze and design logic gates. 5. Ability to identify basic requirements for a design application and propose a cost-effective solution. 6. The ability to understand, analyze and design various combinational circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Understand basic concepts and logic systems. 2. Understand number systems and conversions of number systems. 3. Students will be able to analyze and design logic gates using Boolean algebra and other key concepts. 4. Students will be able to describe the strengths and weaknesses of different system designs and select the appropriate design for a given problem. 5. Students will be able to communicate effectively about their designs, both orally and in writing. 6. Students will be able to understand the principles of combinational circuits.
Indicative Contents المحتويات الإرشادية	**Indicative content includes the following** **Part A – number system and simplification of digital circuit design** Introduction to digital quantities and System Numbers: Decimal, Binary, Binary arithmetic, Octal and Hexadecimal Numbers, Conversions of System Numbers, Arithmetic Operations with different number systems, and Signed Numbers. Digital Codes: Binary coded decimal [BCD], Excess-3 code, Gray codes. Simplification of digital circuit design: Boolean algebra, De'Morgan Theorems, Simplification Using Boolean Algebra, Standard Forms of Boolean Expressions (SOP and POS form), The Karnaugh Map. [21 hrs]. **Part B - Combinational Logic** Flip-Flops: Latches, Edge-Triggered Flip-Flops and its applications. Functions of Combinational Logic: Adders, Subtractors, Parallel Binary Adders, multiplier, and Magnitude comparators. [18 hrs]. Encoders, Decoders, Multiplexers, Demultiplexers. [9 hrs].

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, homework's and examples. Practical examples helps students to understand the course material.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	**78**	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	**5.2**
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	**72**	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	**4.8**
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation
تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	Quizzes	2	10% (5)	6 and 12	LO #1 to #4 and #5 to #6
	Assignments	2	10% (5)	3 and 12	LO #2 to #6
	Projects / Lab.	1	10% (10)		
	Participation & Attendance	1	10% (10)		
Summative assessment	Midterm Exam	2hr	10% (10)	8	LO #1 - #3
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

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Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction to Digital Techniques and logic gates, General number formula: Binary, octal, decimal, hexadecimal numbers
Week 2	Conversions of System Numbers
Week 3	Arithmetic operations with different number systems, complements of number systems, binary codes, BCD codes, Ex-3 code, and Gray code.
Week 4	Logic Gates, Boolean algebra, De'Morgan theorems, Simplification Using Boolean Algebra
Week 5	Standard Forms of Boolean Expressions (SOP and POS form)
Week 6	The Karnaugh Map (two, three, four, and five-variable Karnaugh Maps)
Week 7	Combinational Logic circuit and circuit analysis
Week 8	Midterm Review
Week 9	Adders, Subtractors, Parallel Binary Adders
Week 10	Binary multiplier circuits and Magnitude comparators circuit
Week 11	Flip-Flops:(Latches, Edge-Triggered Flip-Flops) and it's applications
Week 12	Counter and Shift register
Week 13	Encoders and Decoders circuits
Week 14	Multiplexers and Demultiplexers circuit
Week 15	Course Review
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Introduction to logic gates
Week 2	Logic Gates (NOT, AND, NAND)
Week 3	Logic Gates (OR, NOR)
Week 4	Logic Gates (XOR, XNOR)
Week 5	Exercises

Week 6	Universal Gates (NAND, NOR)
Week 7	Combinational Logic circuit
Week 8	Half Adder & Full Adder
Week 9	Half Subtractor & Full Subtractor
Week 10	Even and odd Parity Generator and Checker Circuit
Week 11	Code converter Circuits
Week 12	Flip-Flop
Week 13	Encoder Circuit
Week 14	Decoder Circuit
Week 15	Multiplexer Circuit

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Thomas .L. Floyd, "Digital Fundamentals" . Robert L. Boylestad and Louis Nashelsky, "Electronic Devices and Circuit Theory".	Yes
Recommended Texts	Digital Design, M. Morris. Mano, Pearson prentice Hall .	No
Websites		

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks %	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.