Ministry of Higher Education and
Scientific Research - Iraq
University of Diyala
College of Artificial Intelligence Engineering Technology
Department of Artificial Intelligence Engineering

الملحق 4: وصف المادة الدراسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Principles of Logic Systems**			**Module Delivery**	
Module Type	**Core**			☒**Theory** ☐ **Lecture** ☐ **Lab** ☒**Tutorial** ☐**Practical** ☐**Seminar**	
Module Code	**AIE 105**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	1	
Administering Department	AI Eng.		**College**	College of Artificial Intelligence Engineering Technology	
Module Leader			**e-mail**		
Module Leader's Acad. Title			**Module Leader's Qualification**		
Module Tutor	Name (if available)		**e-mail**	E-mail	
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date			**Version Number**		

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	Digital Logic Circuits Design	**Semester**	2

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	1. To acquire the basic knowledge of Digital systems and applications. 2. To understand and examine the structure of various number systems and its application in digital design. 3. The ability to understand conversion between digital systems. 4. The ability to understand, analyze and design logic gates. 5. Ability to identify basic requirements for a design application and propose a cost-effective solution. 6. The ability to understand, analyze and design various combinational circuits.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Understand basic concepts and logic systems. 2. Understand number systems and conversions of number systems. 3. Students will be able to analyze and design logic gates using Boolean algebra and other key concepts. 4. Students will be able to describe the strengths and weaknesses of different system designs and select the appropriate design for a given problem. 5. Students will be able to communicate effectively about their designs, both orally and in writing. 6. Students will be able to understand the principles of combinational circuits.
Indicative Contents المحتويات الإرشادية	- Introduction to digital quantities and System Numbers [20 hrs] - Arithmetic Operations with different number systems, and Signed Numbers Digital Codes. [8 hrs] - Logic Gates and its applications [4 hrs] - Simplification of digital circuit design [20 hrs] - Introduction to Combinational Logic circuit and its functions [8 hrs]

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, homework's and examples. Practical examples helps students to understand the course material.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	**63**	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	**4**
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	**87**	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	**5.8**
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	**4**	**20% (20)**	**6 and 12**	**LO #1 to #4 and #5 to #6**
	Assignments	**4**	**20% (20)**	**3 and 12**	**LO #2 to #6**
	Projects / Lab.				
	Report				
Summative assessment	**Midterm Exam**	**2hr**	**10% (10)**	**8**	**LO #1 - #3**
	Final Exam	**3hr**	**50% (50)**	**16**	**All**
Total assessment			**100% (100 Marks)**		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Introduction to digital quantities and numbering systems
Week 2	Binary and decimal numbers
Week 3	Octal and hexadecimal numbers
Week 4-5	Conversions between Numbering Systems
Week 6	Arithmetic operations with different number systems, complements of number systems
Week 7	Binary codes, BCD codes, Ex-3 code, and gray code.
Week 8	Logic Gates and its applications
Week 9-10	Boolean Algebra and Logic Simplification
Week 11	Simplification with karnaugh Map
Week 12-13	The karnaugh Map (two, Three, Four and Five- Variable Kamaugh Maps)
Week 14	Introduction to Combinational Logic circuit and circuit analysis
Week 15	Functions of Combinational Logic
Week 16	Preparatory week before the final Exam

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	
Week 2	
Week 3	
Week 4	
Week 5	
Week 6	
Week 7	

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	Digital Fundamentals, Thomas .L. Floyd, Pearson international edition.	Yes
Recommended Texts	Digital Design, M. Morris. Mano, Pearson prentice Hall .	No
Websites		

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.